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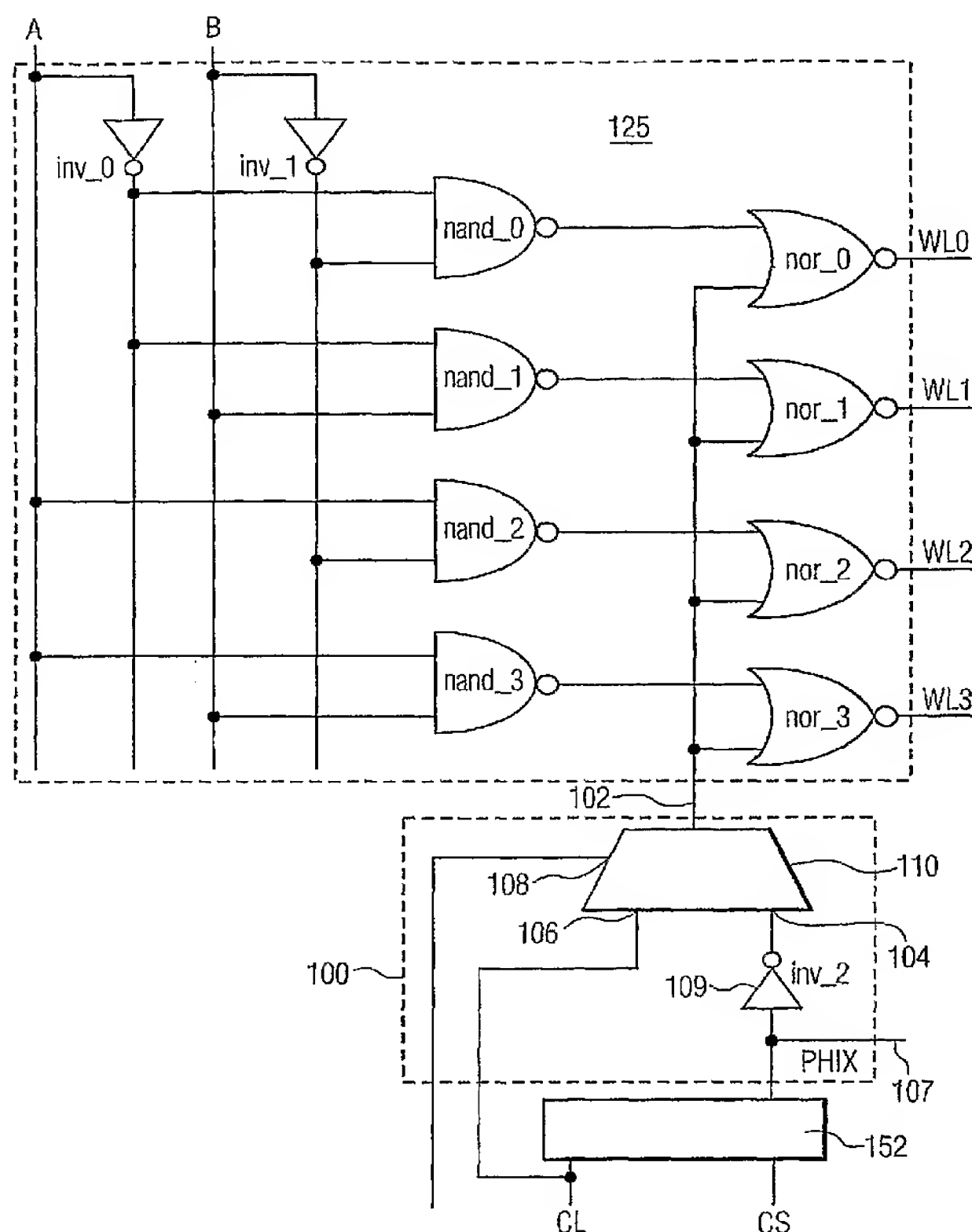
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(54) Title: DFT TECHNIQUE FOR STRESSING SELF-TIMED SEMICONDUCTOR MEMORIES TO DETECT DELAY FAULTS



(57) Abstract: The present invention relates to a test system (100) interposed between a clock monitor (152) and an internal memory block (125) of a self-timed memory. In an example embodiment, the test system (100) receives an internal clock signal (104) from the clock monitor (152), an external clock signal (CL) and a control signal (CS). A multiplexer (110) of the test system provides in dependence upon the control signal (CS) the internal clock signal (104) to the internal memory block (125) during a normal mode of operation of the self-timed memory and the external clock signal (CL) to the internal memory block (125) during a test mode (108) of the self-timed memory. The test system (100) enables control of the clock cycle of the internal memory block (125) by directly applying the external clock signal (CL) during test mode. Thus, the internal memory block is stressed properly enabling the detection of small delay faults.



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